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03500.017818.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	:	Examiner: Not Yet Assigned
YOJI TERAMOTO	)	
	:	Group Art Unit: Not Yet Assigned
Application No.: 10/758,193	)	
	:	
Filed: January 16, 2004	)	
	:	
For: METHOD OF MANUFACTURING ELECTRON-EMITTING DEVICE, METHOD OF MANUFACTURING ELECTRON SOURCE, AND METHOD OF MANUFACTURING IMAGE DISPLAY DEVICE	)	
	:	June 3, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SECOND INFORMATION DISCLOSURE STATEMENT

Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56 and in accordance with the practice under 37 C.F.R. §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed Form PTO-1449. Copies of the listed non-U.S. Patent documents are also enclosed. The documents were cited in a Japanese Official Letter (copy enclosed) issued in a Japanese counterpart of the present application.

The concise explanation of relevance for the non-English documents is provided by the English language abstracts attached thereto. Also, partial English translations of the non-English documents are set forth in this Information Disclosure Statement.

Applicant represents that part of the Japanese Official Letter states as follows (marked as "Remarks A:" and "Remarks B:" by Applicant):

* Remarks A:

See paragraphs [0058] through [0062], [0074] and [0075] and Figs. 9, 11 and 12 of the cited reference 1 (where it is disclosed that thermal oxide film (corresponding to a protective layer) is only wet etched).

Besides, it is no more than conventional means to provide an emitter on the conductive layer.

* Remarks B:

See paragraphs [0058] and [0059] and Fig. 3 of the cited reference 2 (where it is disclosed that a protective layer on the emitter is wet etched).

See paragraphs [0098] through [0100] and Fig. 8 of the cited reference 3 (where it is disclosed that a gate electrode and a convergent electrode are arranged via an insulating layer and both of the electrodes and the insulating layer are etched to form an opening.).

It would be readily conceivable to apply the configuration of an opening being formed in the gate electrode, the convergent electrode and the insulating layer in the invention disclosed in the cited reference 2 instead of the configuration of an opening being formed in the gate electrode and the insulating layer in the invention disclosed in the cited reference 1.

List of the cited references

1. Japanese Patent Application Laid-Open No. 2001-126608
2. Japanese Patent Application Laid-Open No. 2002-140979
3. Japanese Patent Application Laid-Open No. 2000-323013

For the concise statement of relevance of non-English document JP 2002-140979, Applicant represents that paragraphs [0098], [0099] and [0100] of that document state the following:

[0098]

In other words, this FED is similar to that described in Fig. 5 except for the portions described below. Emitter-hole-remaining aluminum 44 adheres to the inner wall of emitter holes 12, as shown in the figure. The manner of adhesion of this emitter-hole-remaining aluminum 44 will be expressed in words. From the top portion to the central portion of the emitter hole inner wall is completely covered with aluminum, and a part of the resin inner wall of the emitter hole is exposed at the emitter hole bottom 45. Here, aluminum of 200 nm in thickness, for example, is deposited by sputtering, a coating of a photoresist is applied, a photoresist of a pattern having a diameter smaller than the emitter diameter by 10% is removed by development, and thereafter, dissolution is performed with an alkaline solution. In this manner, a part of the emitter hole bottom 45 with the end portion in a round shape protruding in an inward direction is dissolved so as

to take the shape shown in the figure, and a cardo resin is exposed at the surface thereof. The aluminum protective film 46 at the emitter hole bottom 45 has been deposited with a thickness of 1 micron in advance of the series of steps described above, and therefore, remains after immersion in the aforementioned alkaline dissolving solution. A part of the cardo resin residue 47 on the aluminum protective film 46 is removed by a lift-off action due to immersion in this alkaline dissolving solution. However, a part of the cardo resin residue 47 remains, as shown in the figure.

[0099]

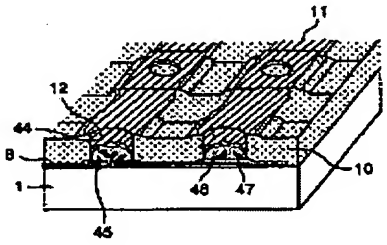
When ashing is performed in this condition with oxygen plasma, the cardo resin residue 47 is burnt off by the ashing. Subsequently, a coating of a photoresist is applied, a photoresist of a pattern having a diameter larger than the emitter diameter by 10% is removed by development, and thereafter, dissolution is performed with an alkaline solution. Aluminum is thereby completely removed from the emitter hole inner wall and the emitter hole bottom 45. Consequently, the CNT in the vicinity of the emitter hole bottom 45 and the gate wiring composed of the gate conductive film 11 are brought into an insulated condition.

[0100]

[Example 13]

In Example 13, the insulation film described in each of the aforementioned Examples is specified to be a photosensitive material (may be an organic photosensitive material). Explanations will be made without using any figure. The case where a gate insulation film is colored at, for example, 300°C can be exemplified.

【図8】



For the concise statement of relevance of non-English document JP 2001-126608, Applicant represents that paragraphs [0058] and [0059] of that document state the following:

[0058]

<Embodiment 3>

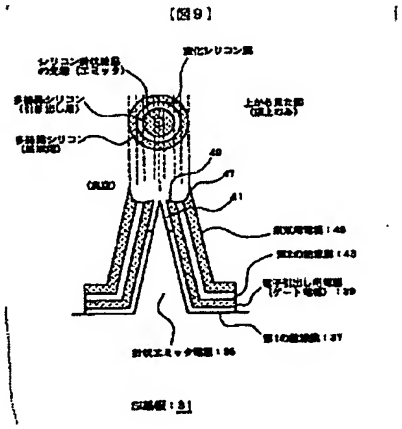
Fig. 9 is a cross sectional view illustrating an electron emitting semiconductor device according to this embodiment. In this embodiment, further improvement is made on the semiconductor device of the above-mentioned embodiments. Here, an electron drawing electrode is provided over the needle-shaped emitter electrode and an electron convergent electrode is further provided thereover.

[0059]

With reference to Fig. 9, the needle-shaped emitter electrode 35 made of silicon needle member protrudes from the silicon substrate 31 into the vacuum.

[FIG. 9]

EDGE OF SILICON NEEDLE-SHAPED CRYSTAL (EMITTER)
POLYCRYSTALLINE SILICON (FOR DRAWING)
POLYCRYSTALLINE SILICON (FOR CONVERGENCE)
(VACUUM)
SILICON NITRIDE FILM
VIEW SEEN FROM THE ABOVE (TOP ONLY)
45: CONVERGENT ELECTRODE
43: SECOND INSULATING LAYER
39: ELECTRON DRAWING ELECTRODE (GATE ELECTRODE)
37: FIRST INSULATING LAYER
35: NEEDLE-SHAPED EMITTER ELECTRODE
31: SI SUBSTRATE



Also, for the concise statement of relevance of non-English document JP 2000-323013, Applicant represents that paragraphs [0098], [0099] and [0100] of that document state the following:

[0098]

[Step-200] First, a cathode electrode 11 is formed on a support 10. Formation of the cathode electrode 11 is performed using a chrome layer in the same way as the embodiment 1. Next, an insulating layer 12 of 0.7 μm in thickness is formed on the support 10 and the cathode electrode 11. Formation of the insulating layer 12 is performed in accordance with the condition shown in Table 3 mentioned above. Then, a gate electrode 13 is formed on the insulating layer 12 in the same way as the embodiment 1.

[0099]

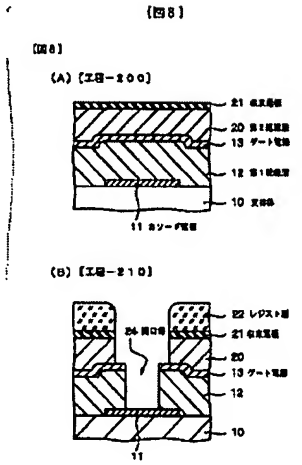
Then, a second insulating layer 20 which is made of SiO_2 and has the thickness of about 1 μm is formed over the whole surface by the CDV method in accordance with the condition shown in Table 3 mentioned above. Further, a tungsten layer of about 0.7 μm in thickness is deposited over the whole second insulating layer 20 by sputtering method, for example in accordance with the condition shown in Table 11 mentioned above, and a predetermined patterning is performed to form a convergent electrode 21.

[0100]

[Step-210] Next, on the second insulating layer 20 including the convergent electrode 21, a resist layer 22 having a predetermined pattern is formed. This resist layer 22 is used as a mask to etch the convergent electrode 21, the second insulating layer 20, the gate electrode 13 and the insulating layer 12 sequentially. By this etching, as shown in Fig. 8(B), a round opening 24 is formed at the bottom with a part of the cathode electrode 11 exposed to. Here, etching of the convergent electrode 21 and gate electrode 13 is performed in accordance with the condition shown in Table 5 mentioned above. Further, etching of the second insulating layer 20 and the insulating layer 12 is performed in accordance with the condition shown in Table 6 mentioned above.

[FIG. 8]
(A) [STEP-200]
21 CONVERGENT ELECTRODE
20 SECOND INSULATING LAYER
13 GATE ELECTRODE
12 FIRST INSULATING LAYER
10 SUPPORT
11 CATHODE ELECTRODE

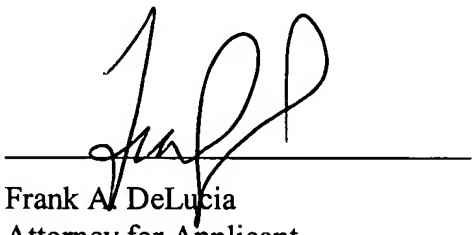
(B) [STEP-210]
24 OPENING
22 RESIST LAYER
21 CONVERGENT ELECTRODE
13 GATE ELECTRODE



It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address given below.

Respectfully submitted,



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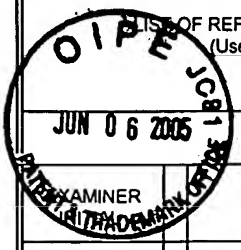
FORM PTO 1449 (*modified*)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT(S)
(Use several sheets if necessary)



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APPLICANT: Yoji Teramoto

FILING DATE	GROUP
January 16, 2004	N.Y.A.

U.S. PATENT DOCUMENTS

EXAMINER		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/ OR ABSTRACT
		2002-140979	05/17/02	Japan			Abstract
		2001-126608	05/11/01	Japan			Abstract
		2000-323013	11/24/00	Japan			Abstract

OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form #62